IN THE CLAIMS

This listing of Claims shall replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A request tracking data prefetch apparatus for a computer system, comprising:

a prefetcher coupled to a high latency memory for a processor of the computer system;

a tracker within the prefetcher and configured to recognize processor accesses to a plurality of cache lines within a low latency memory operable to supply data to the processor responsive to processor data requests, wherein the processor accesses form a stream type sequential access pattern, and wherein further the tracker is configured to use a bit vector to predictively load a target cache line indicated by the stream-type sequential access pattern from the high latency memory into ~~a~~ the low latency memory for the processor in preparation for the target cache line being requested by the processor as part of the stream-type processor access pattern.

2. (Previously Presented) The apparatus of claim 1, wherein the tracker includes a tag configured to recognize accesses to corresponding cache lines of the high latency memory by the processor.

3. (Previously presented) The apparatus of claim 2, wherein a plurality of accesses by the processor to the high latency memory as recognized by the tag are used

by the tracker to determine the target cache line for a predictive load into the low latency memory.

4. (Currently amended) The apparatus of claim 3, wherein consecutive accesses by the processor to adjacent cache lines~~, wherein the adjacent cache lines have adjacent addresses,~~ of the high latency memory are used to determine the target cache line for a predictive load into the low latency memory, and wherein the adjacent cache lines have adjacent addresses.

5. (Original) The apparatus of claim 1, wherein the high latency memory comprises a memory block of a plurality of memory blocks of the computer system.

6. (Previously presented) The apparatus of claim 5, wherein the high latency memory comprises a four kilobyte page of system memory of the computer system.

7. (Previously presented) The apparatus of claim 5, wherein the tracker includes a tag configured to monitor a sub portion of the high latency memory for accesses by the processor.

8. (Original) The apparatus of claim 1, wherein the high latency memory is a system memory of the computer system.

9. (Currently amended) A request tracking data prefetch apparatus for a computer system, comprising:

a processor;

a system memory coupled to the processor;

a prefetch unit coupled to the system memory;

a plurality of trackers included in the prefetch unit, wherein the trackers are respectively configured to recognize processor accesses to pages of the system memory, and configured to recognize accesses to cache lines within a cache memory operable to supply data to the processor responsive to processor data requests that form a stream type sequential access pattern; and

~~a~~ the cache memory coupled to the prefetch unit, wherein the prefetch unit uses a bit vector to predictively load target cache lines from the system memory into the cache memory to reduce an access latency of the processor in preparation for the target cache lines being requested by the processor as part of the stream-type sequential processor access pattern, and wherein the target cache lines are indicated by the stream type sequential access pattern identified by the trackers.

10. (Original) The apparatus of claim 9, wherein each of the trackers include a tag to recognize accesses to cache lines by the processor.

11. (Original) The apparatus of claim 9, wherein a plurality of system memory accesses by the processor are used by the trackers to determine the target cache lines for a predictive load into the cache memory.

12. (Previously presented) The apparatus of claim 11, wherein consecutive accesses by the processor to adjacent cache lines of a page are used to determine the

target cache line for a predictive load into the cache memory, wherein the adjacent cache lines have adjacent addresses.

13. (Original) The apparatus of claim 9, wherein the system memory comprises a plurality of 4KB pages.

14. (Previously presented) The apparatus of claim 9, wherein each of the plurality of trackers is configured to monitor a sub portion of a page for accesses by the processor.

15. (Original) The apparatus of claim 14, wherein the cache lines are 128 byte cache lines and wherein a tag is used to monitor half of a page for accesses by the processor.

16. (Original) The apparatus of claim 9, wherein the cache memory is a prefetch cache memory within the prefetch unit.

17. (Original) The apparatus of claim 9, wherein the cache memory is an L2 cache memory.

18. (Currently amended) A method for request tracking data prefetching for a computer system, comprising:

monitoring data transfers between a high latency memory and a low latency memory coupled to a processor by using a prefetcher, wherein the prefetcher is coupled

to the high latency memory, wherein the low latency memory is a cache memory operable to supply data to the processor responsive to the processor data requests;

using a bit vector to track multiple stream-type sequential processor access patterns between the high latency memory and the low latency memory;

prefetching data from the high latency memory to the low latency memory as indicated by the stream type sequential processor access patterns in preparation for the data being requested by the processor as part of the stream type processor access pattern and reducing a data access latency of the processor of the computer system.

19. (Original) The method of claim 18 wherein the computer system includes a plurality of processors, and wherein each of the processors is coupled to a respective high latency memory and a low latency memory.

20. (Currently amended) The ~~apparatus~~ method of claim 18, wherein consecutive accesses by the processor to adjacent cache lines of the high latency memory are used to determine a target cache line of a stream type access pattern for a prefetching to the low latency memory, wherein the adjacent cache lines have adjacent addresses, and wherein the target cache line is part of stream-type accesses that formed the stream-type access pattern.

21. (Previously Presented) The apparatus of Claim 9, wherein said prefetch unit accesses to system memory are timed to utilize processor-to-system memory idle time.

22. (New) A device for request tracking data prefetching for a computer system, comprising:

means for monitoring data transfers between a high latency memory and a low latency memory coupled to a processor, wherein the low latency memory is a cache memory operable to supply data to the processor responsive to the processor data requests;

means for using a bit vector to track multiple stream-type sequential processor access patterns between the high latency memory and the low latency memory;

means for prefetching data from the high latency memory to the low latency memory as indicated by the stream type sequential processor access patterns in preparation for the data being requested by the processor as part of the stream type processor access pattern and wherein the means for prefetching data is operable to reduce data access latency of the processor of the computer system.

23. (New) The device of claim 22 wherein the computer system includes a plurality of processors, and wherein each of the processors is coupled to a respective high latency memory and a low latency memory.

24. (New) The device of claim 22, wherein consecutive accesses by the processor to adjacent cache lines of the high latency memory are used to determine a target cache line of a stream type access pattern for a prefetching to the low latency memory, wherein the adjacent cache lines have adjacent addresses, and wherein the target cache line is part of stream-type accesses that formed the stream-type access pattern.